

UTILITY PATENT APPLICATION TRANSMITTAL

Only for new nonprovisional applications under 37 CFR 1.53(b)

Attorney Docket No.

217806US2

First Inventor or Application Identifier

Takashi MIYANO et al.

Title

SEMICONDUCTOR INTEGRATED CIRCUIT, SYSTEM BOARD AND
DEBUGGING SYSTEM

Assignee Name: KABUSHIKI KAISHA TOSHIBA

Assignee Address: 1-1, Shibaura 1-chome, Minato-ku, Tokyo, Japan

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO:

Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. ☒ Fee Transmittal Form (e.g. PTO/SB/17)
(Submit an original and a duplicate for fee processing)
2. ☒ Specification Total Sheets **31**
3. ☒ Formal Drawing(s)
(35 U.S.C. 113) Total Sheets **13**
4. ☐ Oath or Declaration Total Pages
 - a. ☐ Newly executed (original or copy)
 - b. ☐ Copy from a prior application (37 C.F.R. §1.63(d))
(for continuation / divisional w/ box 17 completed)
 - i. ☐ DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §1.63(d)(2) and 1.33(b).
5. ☐ CD-ROM or CD-R in duplicate, large table or Computer Program (*Appendix*)
6. ☐ Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
 - a. ☐ Computer Readable Form (CRF)
 - b. Specification or Sequence Listing on:
 - i. ☐ CD-ROM or CD-R (2 copies); or
 - ii. ☐ Paper
 - c. ☐ Statements verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

7. ☐ Assignment Papers (cover sheet & document(s))
8. ☒ Application Data Sheet. See 37 CFR 1.76
9. ☐ 37 C.F.R. §3.73(b) Statement ☐ Power of Attorney
(when there is an assignee)
10. ☐ English Translation Document (if applicable)
11. ☒ Information Disclosure Statement (IDS)/PTO-1449 ☒ Copies of IDS Citations (4)
12. ☐ Preliminary Amendment
13. ☒ White Advance Serial No. Postcard
14. ☒ Certified Copy of Priority Document(s)
(if foreign priority is claimed)
15. ☐ Applicant claims small entity status.
See 37 CFR 1.27
16. ☒ Other: Request for Priority, Statement of Relevancy

17. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below:

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application no.:

Prior application information: Examiner:

Group Art Unit:

For CONTINUATION OR DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

18. Amend the specification by inserting before the first line the sentence:

- ☐ This application is a ☐ Continuation ☐ Division ☐ Continuation-in-part (CIP)
of application Serial No. Filed on
- ☐ Which was published in English
- ☐ Which was not published in English
- ☐ This application claims priority of provisional application Serial No. Filed

19. CORRESPONDENCE ADDRESS



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Name:	C. Irvin McClelland	Registration No.:	

Registration Number 21,124

Docket No. 217806US2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

INVENTOR(S) Takashi MIURA, et al.

SERIAL NO: New Application

FILING DATE: Herewith

FOR: SEMICONDUCTOR INTEGRATED CIRCUIT, SYSTEM BOARD AND DEBUGGING SYSTEM

FEE TRANSMITTAL

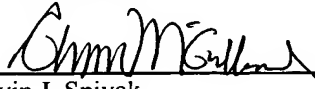
ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

FOR	NUMBER FILED	NUMBER EXTRA	RATE	CALCULATIONS
TOTAL CLAIMS	22 - 20 =	2	× \$18 =	\$36.00
INDEPENDENT CLAIMS	3 - 3 =	0	× \$84 =	\$0.00
<input type="checkbox"/> MULTIPLE DEPENDENT CLAIMS (If applicable)			+ \$280 =	\$0.00
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TOTAL OF ABOVE CALCULATIONS				\$906.00
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- ☐ Please charge Deposit Account No. 15-0030 in the amount of A duplicate copy of this sheet is enclosed.
- ☒ A check in the amount of **\$906.00** to cover the filing fee is enclosed.
- ☒ The Commissioner is hereby authorized to charge any additional fees which may be required for the papers being filed herewith and for which no check is enclosed herewith, or credit any overpayment to Deposit Account No. 15-0030. A duplicate copy of this sheet is enclosed.

Respectfully Submitted,

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Takashi MIURA, et al.

SERIAL NO.: New Application

FILED: Herewith

FOR: SEMICONDUCTOR INTEGRATED CIRCUIT, SYSTEM BOARD AND
DEBUGGING SYSTEM

STATEMENT OF RELEVANCY

Reference AO (3-268159) on Form PTO-1449:

A multi-cpu type device has a similar selector circuit, which selects a pair of serial lines for debugging. And the serial line is connected to the bus by serial parallel converting circuit. (Fig. 1-30, Fig. 1-11, Fig. 1-13)

Reference AP (2752592) on Form PTO-1449:

This processor has a similar Internal-Debugging-Interference and the interface has connected the Debug- Support Unit with the Debug-Module.

Reference AQ (8-185336) on Form PTO-1449:

This reference relates to a microprocessor with debug function.